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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PORTKA, GARY J	

ART UNIT	PAPER NUMBER
2188	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/823,472	Applicant(s) WILLIS ET AL.	
	Examiner Gary J Portka	Art Unit 2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30 and 35-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30 and 35-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the appeal brief filed on May 11, 2004, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

2. Claims 31-34 were canceled in the amendment submitted February 4, 2004. Claims 1-30 and 35-46 are pending.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-30 and 35 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 1, 9, 13, 20, and 35 substantially recite identifying if a virtual address

translation is sharable transparent to the operating system. The disclosure shows sharing indications 1) at 616-618 of Fig. 6, or 2) at 705 and 706 of Figs. 7a and 7b. Obviously these sharing indications must be compared with something that is input in order to determine if the input comes from a processor that is allowed to share the translation (specification pg. 14 lines 7-11, pg. 18 lines 14-17). The only mechanism shown for this is in Fig. 8 at PID (described at page 21 paragraph 0052). Since this PID is disclosed as a logical processor, it is not necessarily generated by hardware, but rather may be set by the process or by some other software mechanism. How it is generated is apparently not disclosed. Applicant has stated that the operating system must be modified to support an equivalent process identifier such as in Bourekas (the arguments refuting the rejection over Bourekas, pgs. 7-9 of the brief). However, it has not been shown how the present invention prevents the requirement to modify the operating system to set and submit the PID and thus how to make the identification of the sharability of the translation transparent to the operating system. Claims 2-8, 10-12, 14-19, and 21-30 depend from claims 1, 9, 13, and 20 respectively, and incorporate the limitations thereof.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-30 and 35 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1, 9, 13, 20, and 35 substantially recite identifying if a virtual address translation is sharable transparent to the operating

system. The disclosure appears to assign this substantially a negative limitation meaning; that is, it means *without requiring special operating system support or modifications* (page 7), or *without requiring the operating system to actively manage the sharing* (page 17). However, this definition does not adequately establish the metes and bounds desired by the claim language, since it is not clear what exactly is meant by "special support" and "actively manage", or whether either of both of these definitions must be met. It is also not clear which operating system is referred to; for example the claims could hypothetically be rejected by simply finding any operating system that is not required to be modified or otherwise support or actively manage an address translation sharing indication (for example in another computer). Claims 2-8, 10-12, 14-19, and 21-30 depend from claims 1, 9, 13, and 20 respectively, and incorporate the limitations thereof.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-30 and 35-46 are rejected under 35 U.S.C. 102(e) as being anticipated by Bourekas, U.S. Patent 6,598,050 B1.

9. As to claims 1-3, 5-10, and 12, Bourekas discloses a method, executable code, and processor for transparently sharing virtual address translations, by accessing a translation and identifying if it is sharable (see Abstract, Figs 1 and 2, col. 1 line 49 to col. 2 line 50, and col. 4 line 21 to col. 5 line 12; the global bit 115 and group membership fields 118 identify if the translation is sharable and if so by the current task, and this procedure is transparent to the OS as recited, since the prior art required OS traps but the invented system requires no traps and therefore no modification of or special support by the OS). This virtual address translation in general does not require OS support except during a page fault, the virtual address is supplied by the program/process and is translated by the hardware. See Tanenbaum, "Modern Operating Systems", where it is described that processes call the operating system using trap instructions (pgs. 16-19), that in paging in general a process generates a virtual address which is translated by the hardware and only requires an OS call upon a page fault (pgs. 89-92 and 105). It is therefore appears incorrect to state that the OS must be modified to support a group membership field with the virtual address, for any particular access request this is entirely supplied by the process, and the virtual address and group membership field comparisons are done in hardware (in the TLB of Bourekas, or if missed in a page table). However, it is certainly incorrect to state that the OS must provide special support or actively manage the sharing of the translation, since it is not involved in routine translations (only at a page fault), and Bourekas further expressly states removing the requirement for trapping to the OS for the control of sharing translations.

10. As to claims 13-15, 19-22, and 28-30, Bourekas discloses processors and multiple logical processors as recited, since multiple tasks/processes are described.

11. As to claim 36, Bourekas discloses a multithreading processor comprising address translation stage with TLB 110 having plurality of entries to translate virtual to physical addresses (one entry shown in Fig. 1), first entry to translate a first virtual address for a first process, control logic comprising circuitry to identify sharability of the first entry (since a circuit must enter/read the G bit 115 to determine if the entry may be shared by all tasks) and to provide a first sharing indication if the first entry may be shared by a second process (since a circuit must enter/read the GRP field 118 and compare it with an incoming request field 107), and sharing indication field (at 118) in the first entry to store the first sharing indication (see Abstract, Figs 1 and 2, col. 1 line 49 to col. 2 line 50, and col. 4 line 21 to col. 5 line 12).

12. As to claims 24-27, 35, 40, and 42-46, Bourekas discloses that the TLB stores the indication (Fig. 1).

13. As to claims 4, 11, 37-38, and 41, in Bourekas the fields 118 identify the logical processes.

14. As to claims 23 and 29, Bourekas discloses the recited matching of second translation data to first since as shown in Fig. 4, multiple matches are performed which result in the recited identification of sharing.

15. As to claims 16-18, Bourekas discloses that the translations provide access to a shared cache, since as shown in Fig. 4 the translations whether to access main memory

238 or the cache 236, and the cache is shared since multiple tasks are performed in the depicted translation procedure.

16. As to claim 39, Bourekas discloses the comparison of the virtual address of any input process with the entries, and therefore inherently circuitry and state machine processes to the extent recited.

17. Claims 1-30 and 35-46 are rejected under 35 U.S.C. 102(e) as being anticipated by Kakeda et al., U.S. Patent 6,564,311 B2.

18. As to claims 1-3, 5-10, and 12, Kakeda discloses a method, executable code, and processor for transparently sharing virtual address translations, by accessing a translation and identifying if it is sharable (see Abstract, Figs 1 and 2, col. 1 lines 10-15, col. 1 line 65 to col. 2 line 65, col. 4 lines 33-65, col. 5 lines 15-23 and 47-59, and col. 7 lines 1-10); the global bits 103 identify if the translation is sharable and if so, in conjunction with PID 102, if so by the current task PID 2, and this procedure is transparent to the OS as recited, since the PID 2 is supplied by the process without regard to the virtual address, or the OS.

19. As to claims 13-15, 19-22, and 28-30, Kakeda discloses processors and multiple logical processors as recited, since multiple tasks/processes are described.

20. As to claim 36, Kakeda discloses a multithreading processor comprising address translation stage with TLB 1 having plurality of entries to translate virtual to physical addresses (entries shown at e1, etc., Fig. 1), first entry to translate a first virtual address for a first process, control logic comprising circuitry to identify sharability of the first entry (including 13 and 105, Fig. 1, 2) and to provide a first sharing indication if the first entry

may be shared by a second process (since a circuit must enter as well as read the PID field 102 and compare it with an incoming request PID at 2), and sharing indication field 102 in the first entry to store the first sharing indication (see Abstract, Figs 1 and 2, col. 1 lines 10-15, col. 1 line 65 to col. 2 line 65, col. 4 lines 33-65, col. 5 lines 15-23 and 47-59, and col. 7 lines 1-10).

21. As to claims 24-27, 35, 40, and 42-46, Kakeda discloses that the TLB stores the indication (Fig. 1).

22. As to claims 4, 11, 37-38, and 41, in Kakeda the fields 118 identify the logical processes.

23. As to claims 23 and 29, Kakeda discloses the recited matching of second translation data to first since as shown in Fig. 4, multiple matches are performed which result in the recited identification of sharing.

24. As to claims 16-18, Kakeda discloses that the translations provide access to a shared cache, since as shown in Fig. 4 the translations whether to access main memory 238 or the cache 236, and the cache is shared since multiple tasks are performed in the depicted translation procedure.

25. As to claim 39, Kakeda discloses the comparison of the virtual address of any input process with the entries, and therefore inherently circuitry and state machine processes to the extent recited.

Response to Arguments

26. Applicant's arguments filed in the brief of May 11, 2004 have been fully considered but they are not persuasive. Applicants argue that in Bourekas the address

translation sharability is not indicated transparent to the operating system because Bourekas states the OS "can support three levels of access in a virtual to physical address translation", and "permits" these translations. However, neither this nor anything else in the reference requires the operating system to be modified or otherwise provide special support or actively manage the sharing of the translation, as required by the apparent definition of "transparent" in the claims. Since it has not been disclosed that the OS has been modified, it in fact is implied that the intention is that the use of the group membership field is compatible with an existing OS; the reference would otherwise be non-enabling if it was assumed that the OS must somehow be modified but exactly how was not disclosed. Applicants argue that if Bourekas did not provide an OS modified to support virtual addresses having group membership fields, there is no alternative method disclosed to permit sharing of address translations. Examiner disagrees that the OS is modified as previously argued; further, alternative methods are disclosed in that the sharability may be determined 1) by group membership field bits, 2) by the field indicating a number of a task, and 3) by an address range comparison. Even if the OS were modified to use the field in cases 1 and 2, in case 3 there is no such need because only the address need be known, then compared in the TLB to the range to determine the group. Applicants argue the Bourekas provides no OS transparent method of determining if translations are NOT sharable since an OS that does not support the group membership field might cause an erroneous reading of the virtual address. Since the hypothesizing of a circumstance where the OS might not be able to correctly handle an address translation does not prove the reverse (that the OS

must be modified to correctly handle it), this argument is moot. Applicants also argue that in Bourekas the group membership bits stored in the TLB are not produced and provided by control logic, but rather by the OS. Examiner responds that even if they were provided by the OS (but which is disputed hereinabove) that would read on control logic since logic in general may be implemented as operations/software; however, even the OS must interface with hardware and that circuit could be considered the control logic. Applicants finally argue basically that Bourekas does not teach the limitations of claim 36, and in response the rejection thereof has been detailed better hereinabove.

Conclusion

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary J Portka whose telephone number is (703) 305-4033. The examiner can normally be reached on M-F 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 305-3900.

Gary J Portka
Primary Examiner
Art Unit 2188

July 16, 2004